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100

110

195
LAYOUT
DATABASE

| 120 BLOCK FLOORPLANNER | 130 BLOCK PLACER |
| 135 LOGIC SYNTHESIZER | 140 ROUTING SPACE ESTIMATOR |

150
CHIP
FLOORPLANNER

| 170 STANDARD CELL PLACER | 160 GLOBAL/DETAIL ROUTER |
| 180 LOGIC SYNTHESIZER | 190 HDL EDITOR |

DISPLAY

191

1/0 DEVICES

192
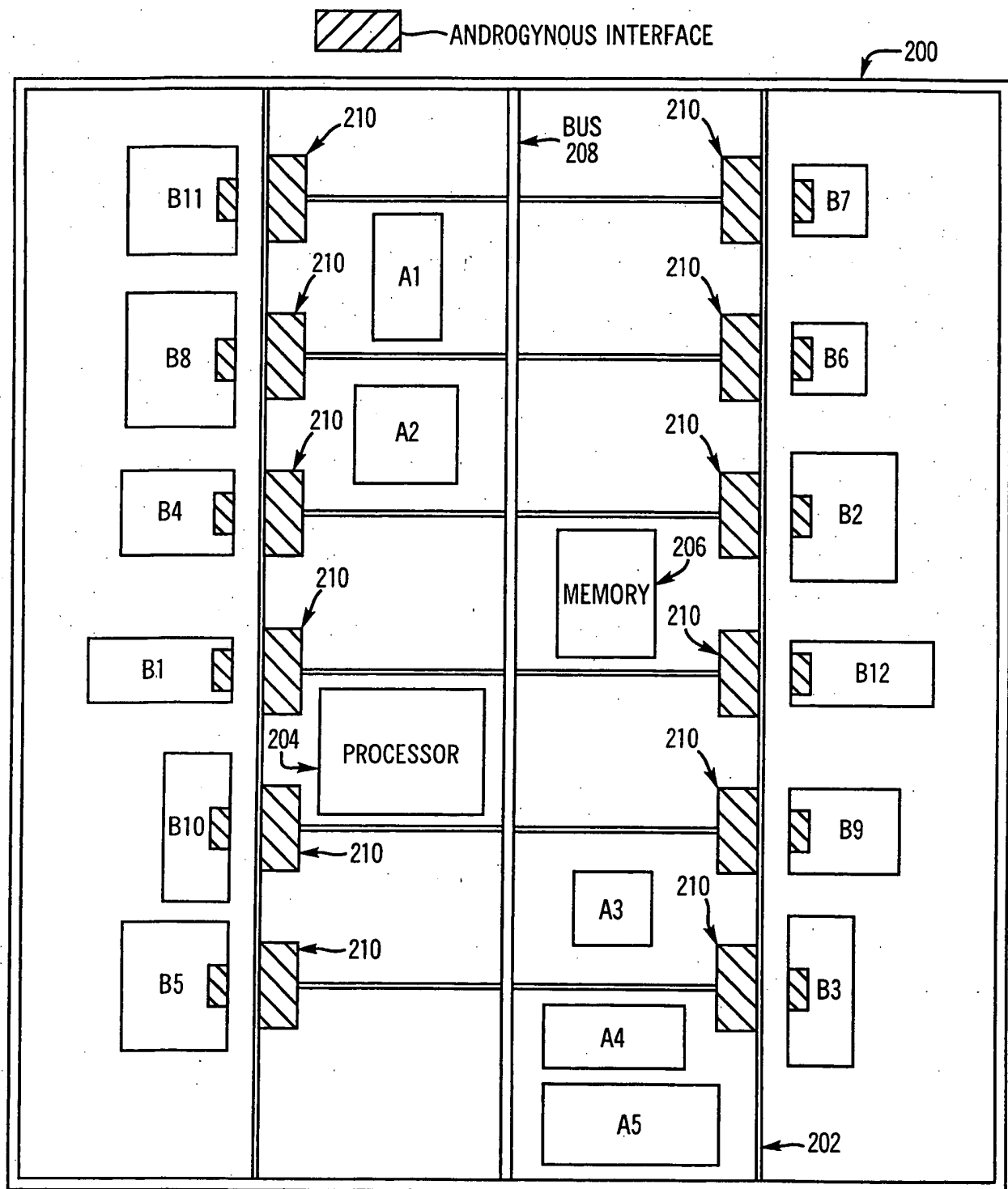
FIG. 1.

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FIG. 2A.

ANDROGYNOUS INTERFACE ~200

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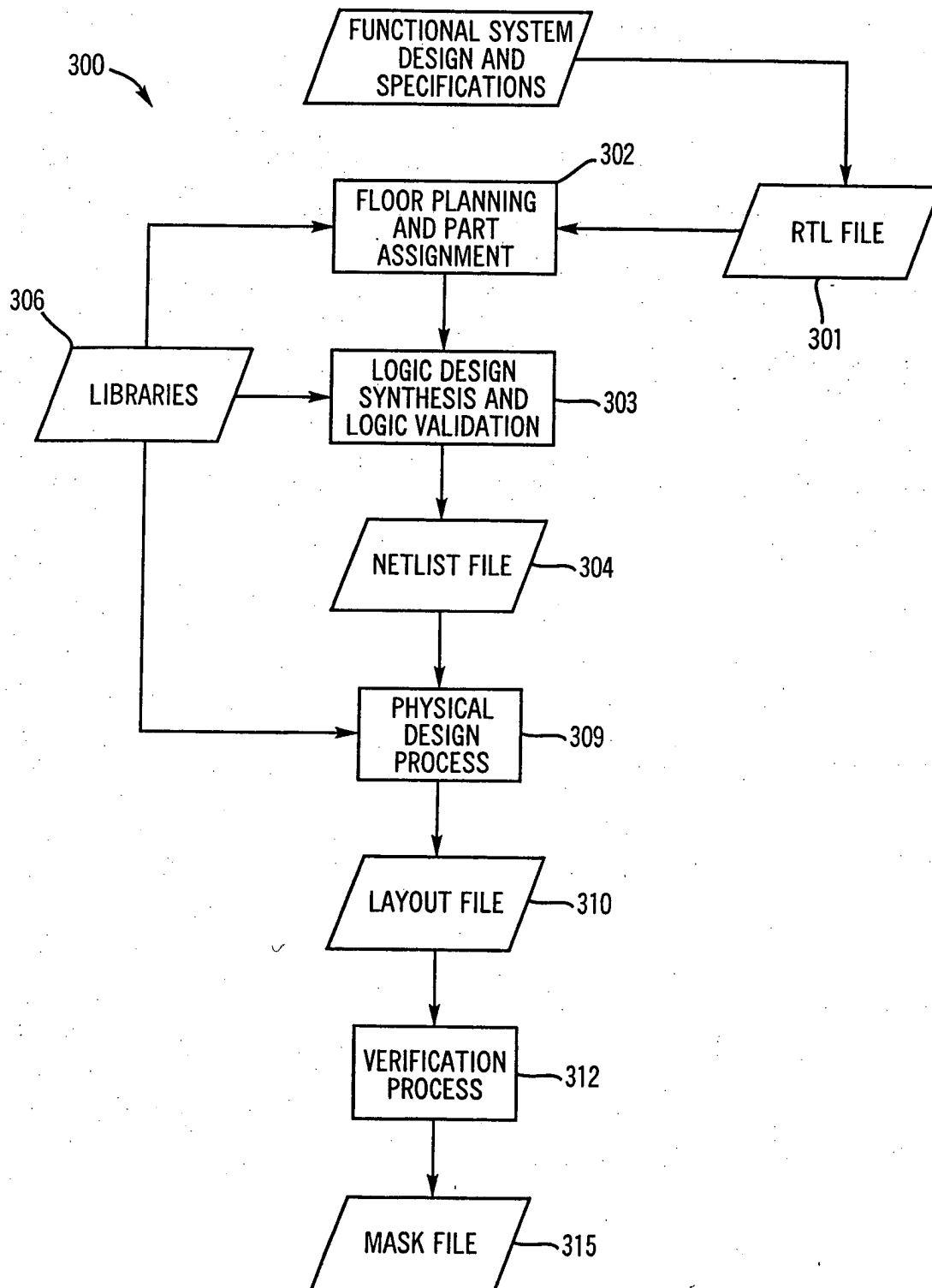FIG. 2B.

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FIG. 3.

300

FUNCTIONAL SYSTEM
DESIGN AND
SPECIFICATIONS

FLOOR PLANNING
AND PART
ASSIGNMENT — 302

RTL FILE

301

LIBRARIES — 306

LOGIC DESIGN
SYNTHESIS AND
LOGIC VALIDATION — 303

NETLIST FILE — 304

PHYSICAL
DESIGN
PROCESS — 309

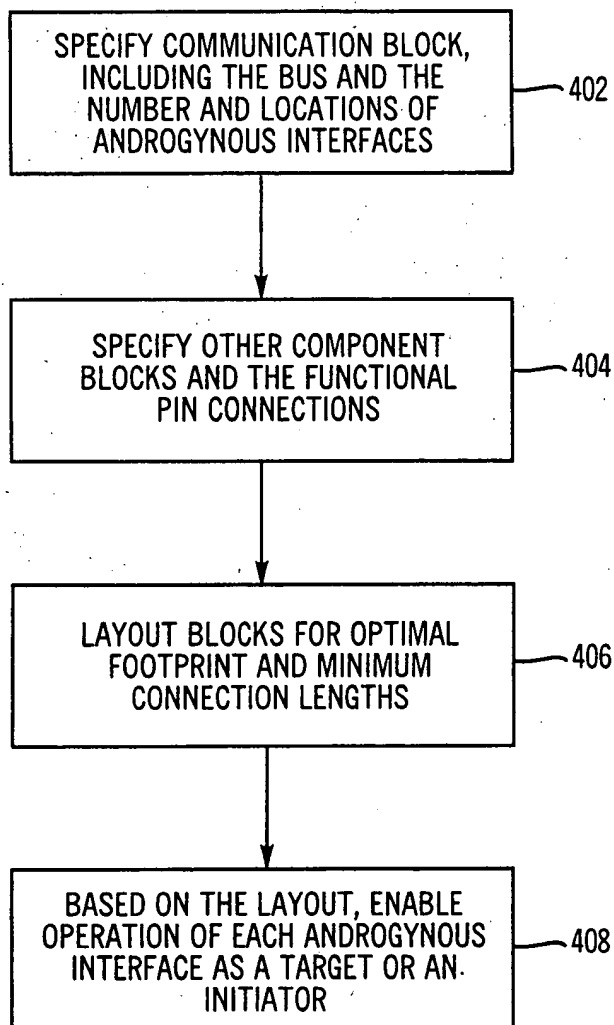LAYOUT FILE — 310

VERIFICATION
PROCESS — 312

MASK FILE — 315

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400

```
┌─────────────────────────────┐
│  SPECIFY COMMUNICATION BLOCK,│
│   INCLUDING THE BUS AND THE  │ ── 402
│   NUMBER AND LOCATIONS OF    │
│    ANDROGYNOUS INTERFACES    │
└─────────────────────────────┘
               │
               ▼
┌─────────────────────────────┐
│   SPECIFY OTHER COMPONENT    │
│  BLOCKS AND THE FUNCTIONAL   │ ── 404
│       PIN CONNECTIONS        │
└─────────────────────────────┘
               │
               ▼
┌─────────────────────────────┐
│   LAYOUT BLOCKS FOR OPTIMAL  │
│    FOOTPRINT AND MINIMUM     │ ── 406
│      CONNECTION LENGTHS      │
└─────────────────────────────┘
               │
               ▼
┌─────────────────────────────┐
│   BASED ON THE LAYOUT, ENABLE│
│ OPERATION OF EACH ANDROGYNOUS│ ── 408
│  INTERFACE AS A TARGET OR AN │
│          INITIATOR           │
└─────────────────────────────┘
```

FIG. 4.

Replacement Sheet
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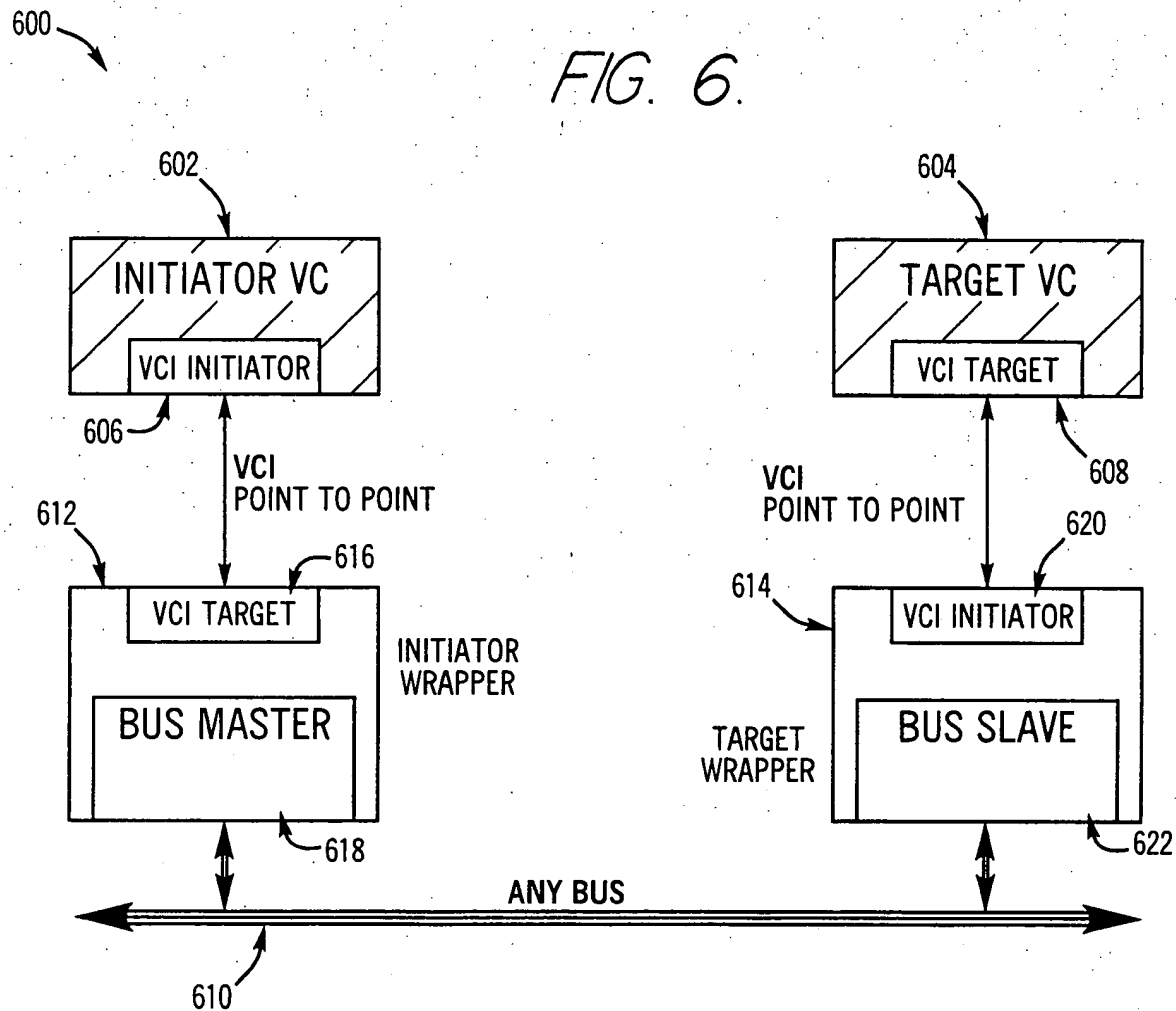Title: Interface Configurable For Use With Target /
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I/T		T/I
R_data	<-	Data
R_addr	<-	Addr
R_cmd	<-	Cmd
R_Plen	<-	Plen
R_Cfix	<-	Cfix
R_Clen	<-	Clen
R_dval	<-	Dval
ACK	->	R_Ack
R_eop	<-	Eop
R_error	<-	Error
Data	->	R_Data
Addr	->	R_Addr
Cmd	->	R_Cmd
Plen	->	R_Plen
Cfix	->	R_Cfix
Clen	->	R_Clen
Dval	->	R_Dval
R_Ack	<-	Ack
Eop	->	R_Eop
Error	->	R_Error

FIG. 5.

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FIG. 6.

600

602

604

```
┌─────────────────────┐          ┌─────────────────────┐
│   INITIATOR VC      │          │    TARGET VC        │
│  ┌───────────────┐  │          │  ┌───────────────┐  │
│  │ VCI INITIATOR │  │          │  │  VCI TARGET   │  │
│  └───────────────┘  │          │  └───────────────┘  │
└─────────────────────┘          └─────────────────────┘
```

606

608

VCI
POINT TO POINT

VCI
POINT TO POINT

612

620

616

614

```
┌─────────────────────┐          ┌─────────────────────┐
│  ┌───────────────┐  │          │  ┌───────────────┐  │
│  │  VCI TARGET   │  │          │  │ VCI INITIATOR │  │
│  └───────────────┘  │          │  └───────────────┘  │
│   INITIATOR         │          │                     │
│   WRAPPER           │          │                     │
│  ┌───────────────┐  │          │  ┌───────────────┐  │
│  │  BUS MASTER   │  │  TARGET  │  │   BUS SLAVE   │  │
│  │               │  │  WRAPPER │  │               │  │
│  └───────────────┘  │          │  └───────────────┘  │
└─────────────────────┘          └─────────────────────┘
```

618

622

ANY BUS

610

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SOC MASTER		VCI SLAVE	VCI MASTER		SOC SLAVE
BCLK	= =	CLOCK	CLOCK	= =	BCLK
BnRES	= =	RESETN	RESETN	= =	BnRES
r_gnt	<-	CMDACK	CMDACK	<-	gnt
r_req	->	CMDVAL	CMDVAL	->	req
r_addr	->	ADDR[n-1:0]	ADDR[n-1:0]	->	addr
1111	->	BE[b-1:0|0:b-1]	BE[b-1:0|0:b-1]	->	xxxx
0	->	CFIXED	CFIXED	->	x
0	->	CLEN[q-1:0]	CLEN[q-1:0]	->	x
r_cmd	->	CMD[1:0]	CMD[1:0]	->	cmd
1	->	CONTIG	CONTIG	->	x
r_data	->	WDATA[8b-1:0]	WDATA[8b-1:0]	->	data
r_eop	->	EOP	EOP	->	eop
0	->	CONST	CONST	->	x
r_d_size	->	PLEN[k-1:0]	PLEN[k-1:0]	->	d_size
0	->	WRAP	WRAP	->	x
gnt	->	RSPACK	RSPACK	->	r_gnt
req	<-	RSPVAL	RSPVAL	<-	r_req
data	<-	RDATA [8b-1:0]	RDATA [8b-1:0]	<-	r_data
eop	<-	REOP	REOP	<-	r_eop
error	<-	RERROR	RERROR	<-	r_error

FIG. 7

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FIG. 8